

100

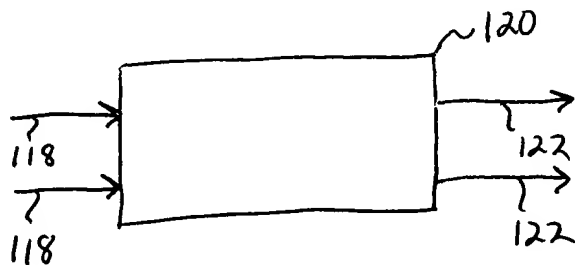
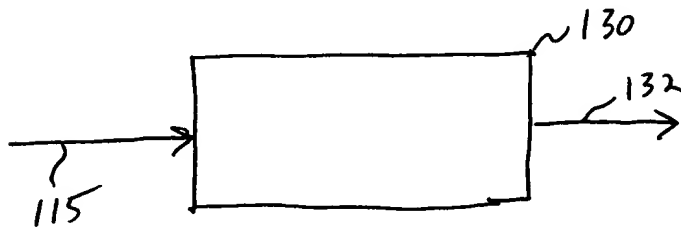
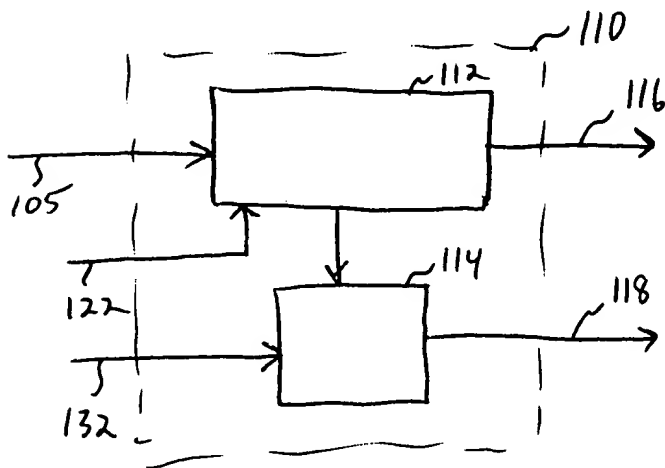
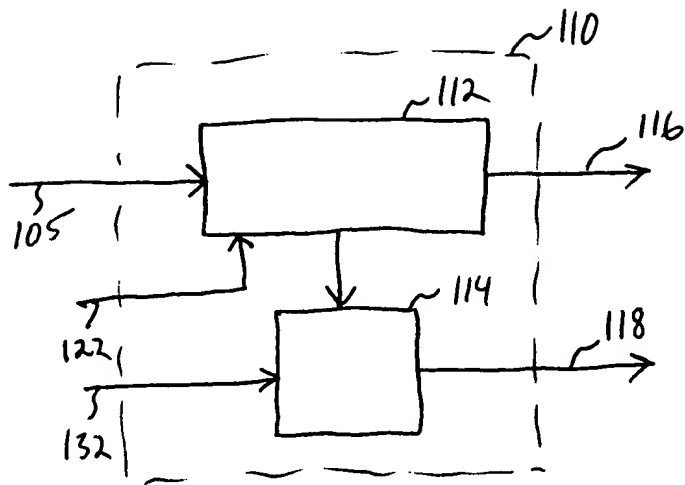


Fig. 1

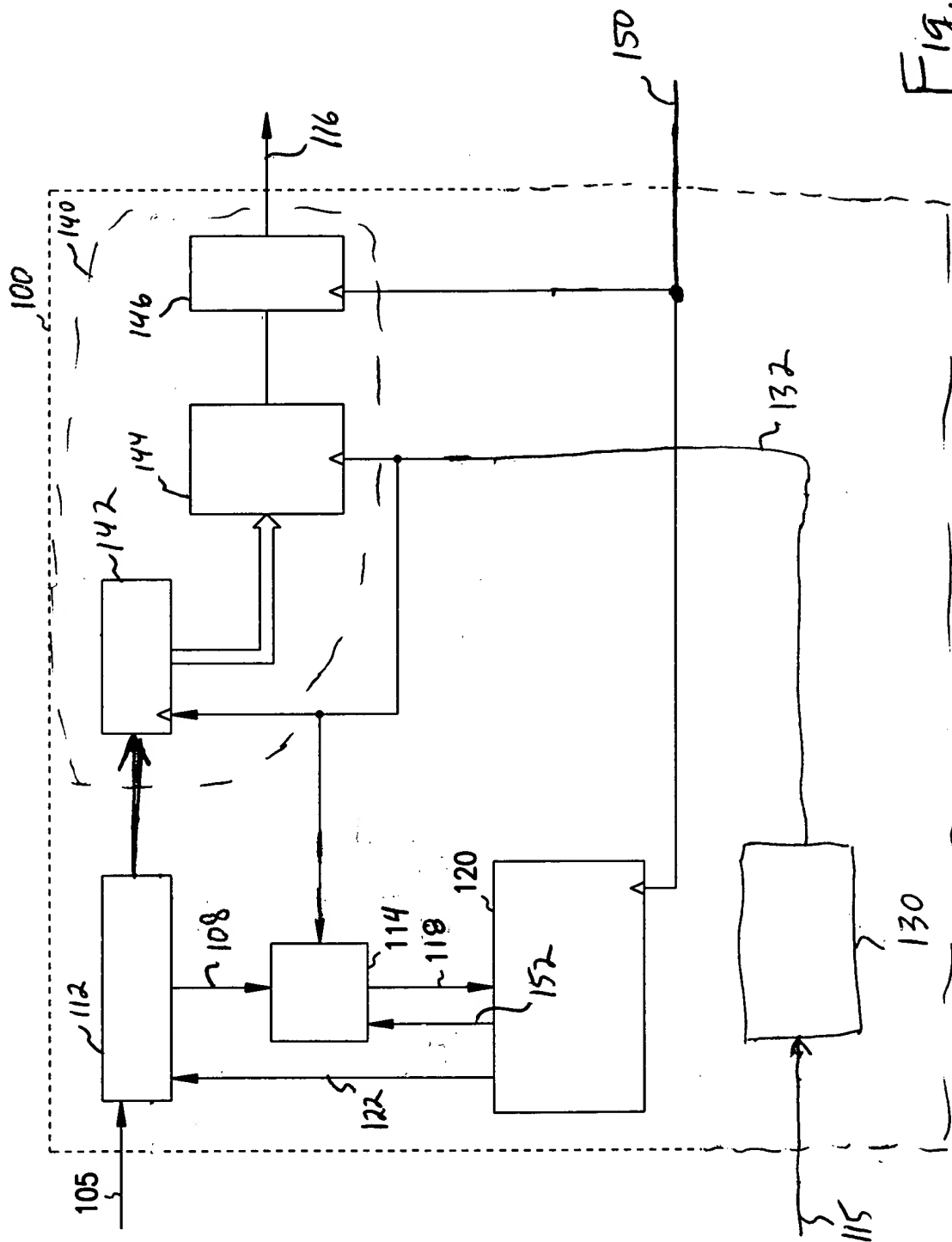


Fig. 2

FIG. 3 is a block diagram of a delay line circuit 100. The circuit 100 includes a Channel Clock input 115, a Fine Tune Delay Line block 160, a CLK 2X block 164, a fanout block 166, a duty cycle sense block 168, and a Delay Line Controller block 120. The Channel Clock input 115 is connected to the Fine Tune Delay Line block 160. The output of the Fine Tune Delay Line block 160 is connected to the CLK 2X block 164. The output of the CLK 2X block 164 is connected to the fanout block 166. The output of the fanout block 166 is connected to the duty cycle sense block 168. The duty cycle sense block 168 is connected to the Delay Line Controller block 120. The Delay Line Controller block 120 has inputs for core\_clk, update, and reset, and outputs for sample and shift\_mode[2:0,4:10].

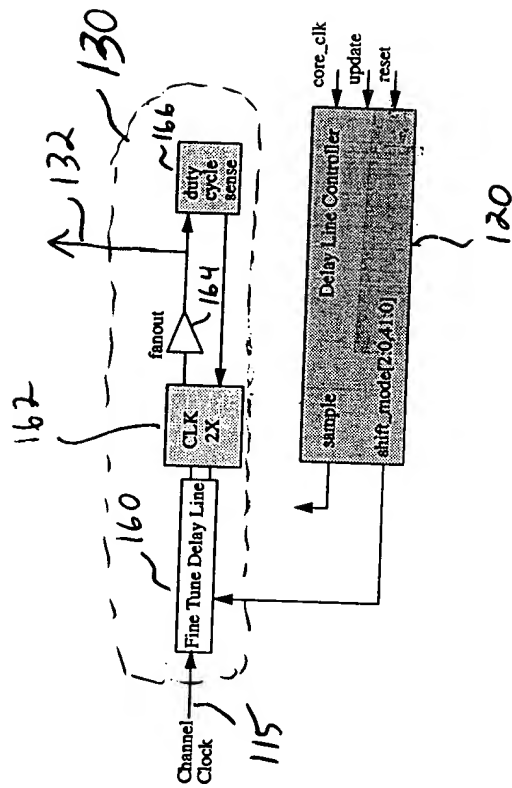


Fig. 3

100

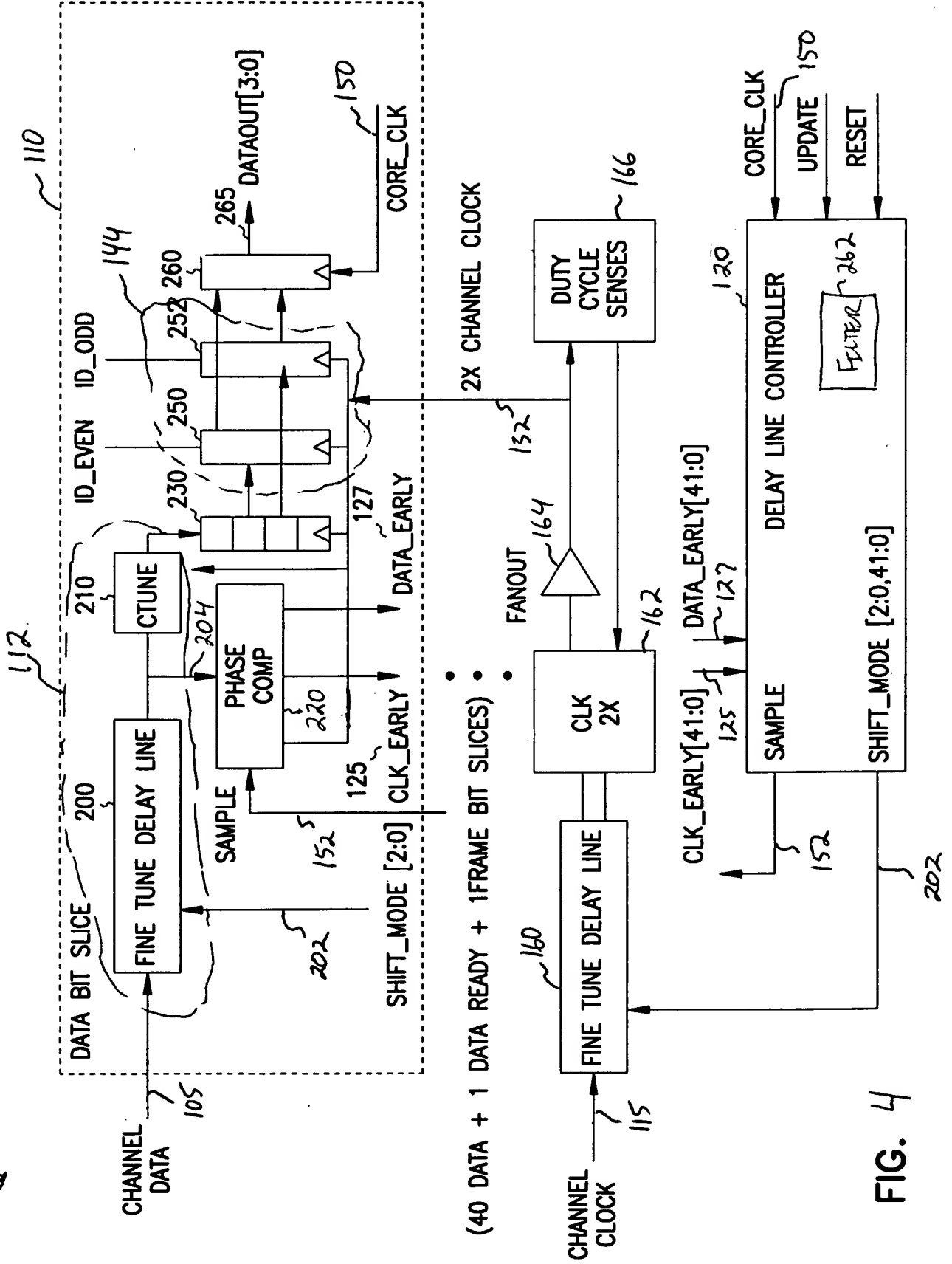


FIG. 4

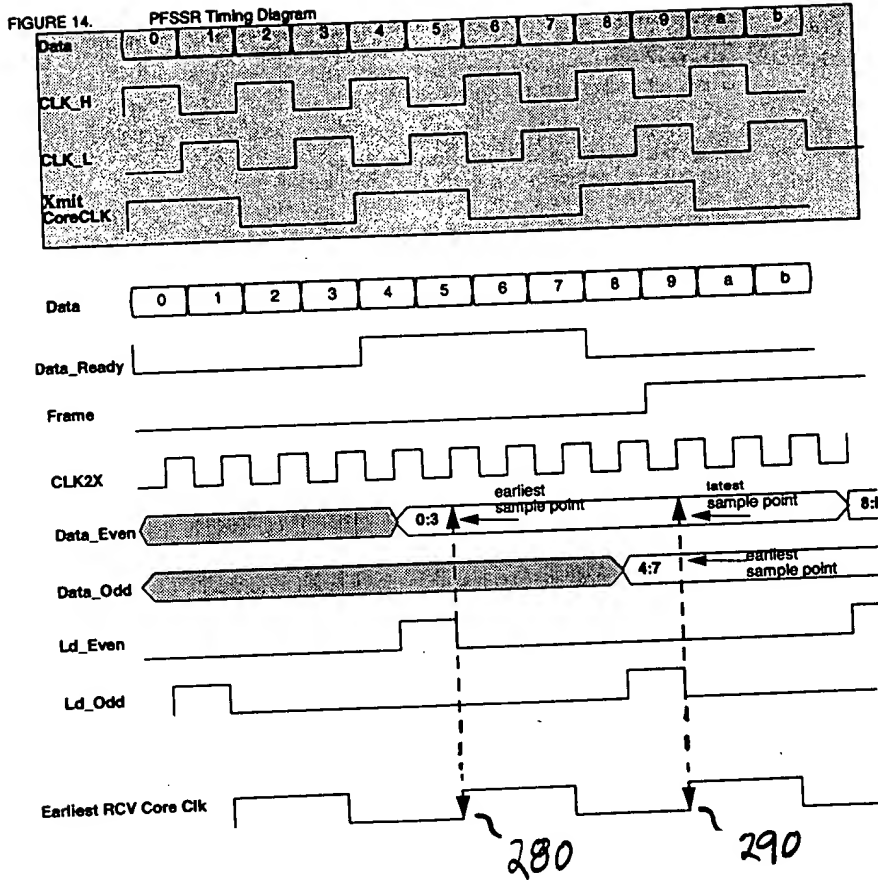


Fig. 5

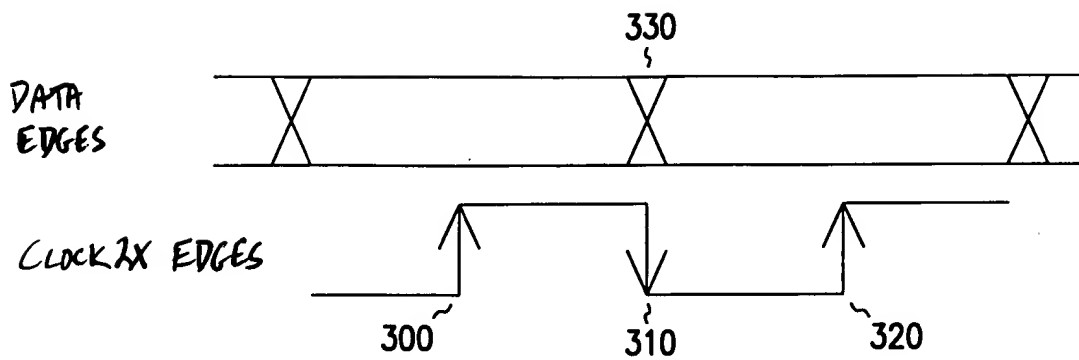


FIG. 6

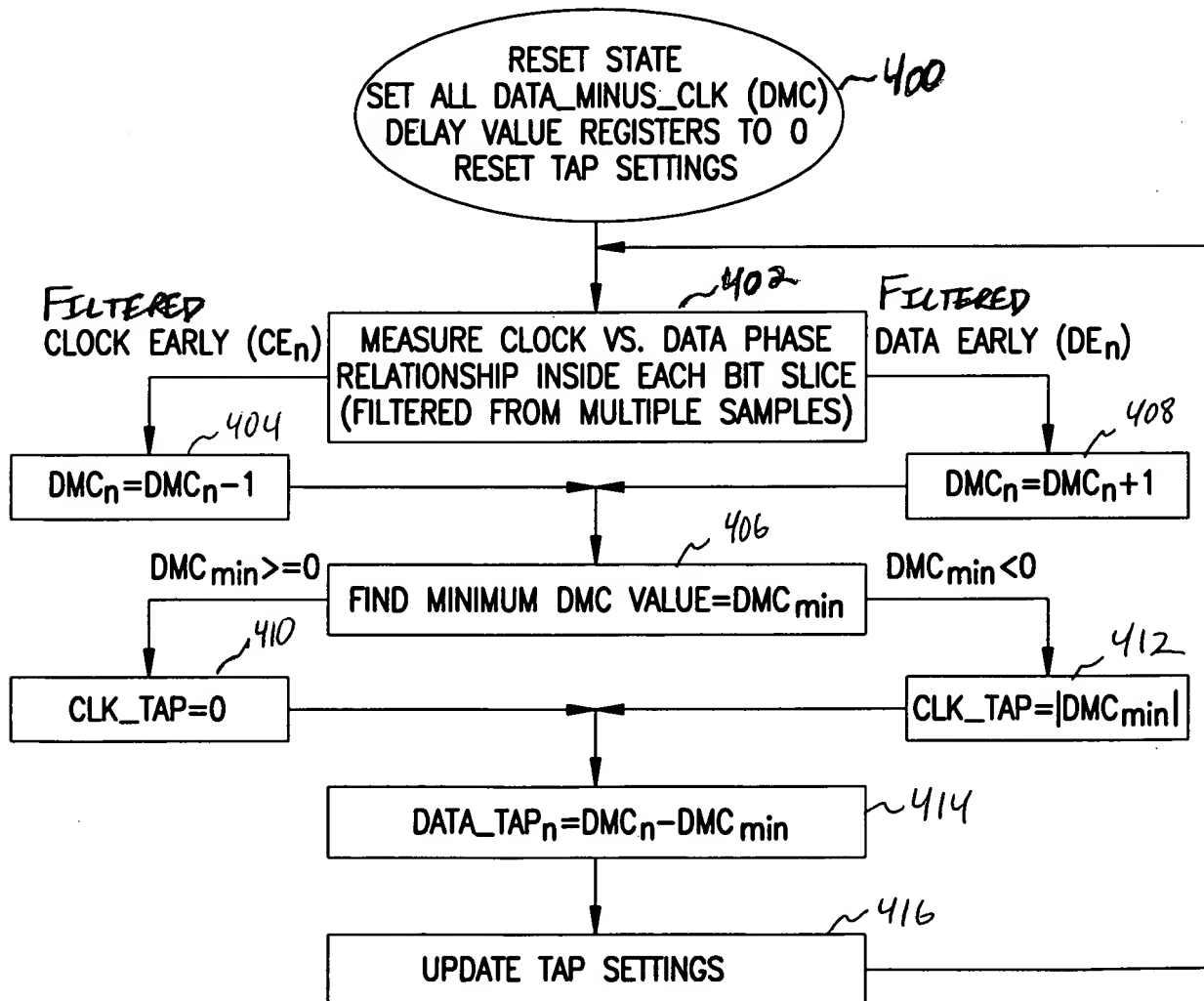


FIG. 9

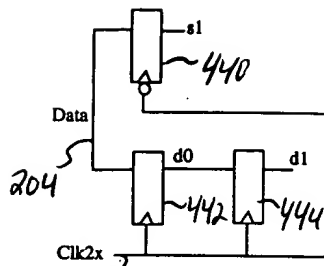


Fig. 8a

Possible Samples - condition

d1	s1	d0	condition
0	0	0	steady 0 (no timing info.)
0	0	1	rising data (clk early)
0	1	0	(uncertain sample)
0	1	1	rising data (data early)
1	0	0	falling data (data early)
1	0	1	(uncertain sample)
1	1	0	falling data (clk early)
1	1	1	steady 1 (no timing info.)

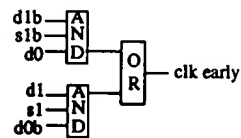


Fig. 8b

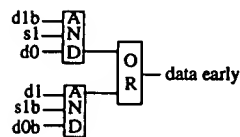


Fig. 8c

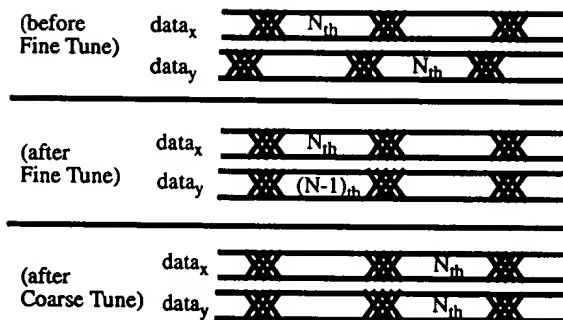


Fig. 7

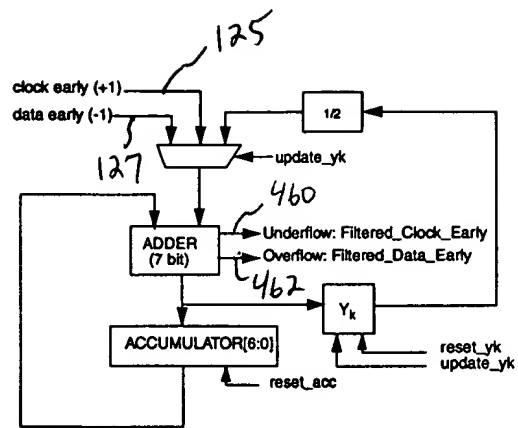


Fig. 10



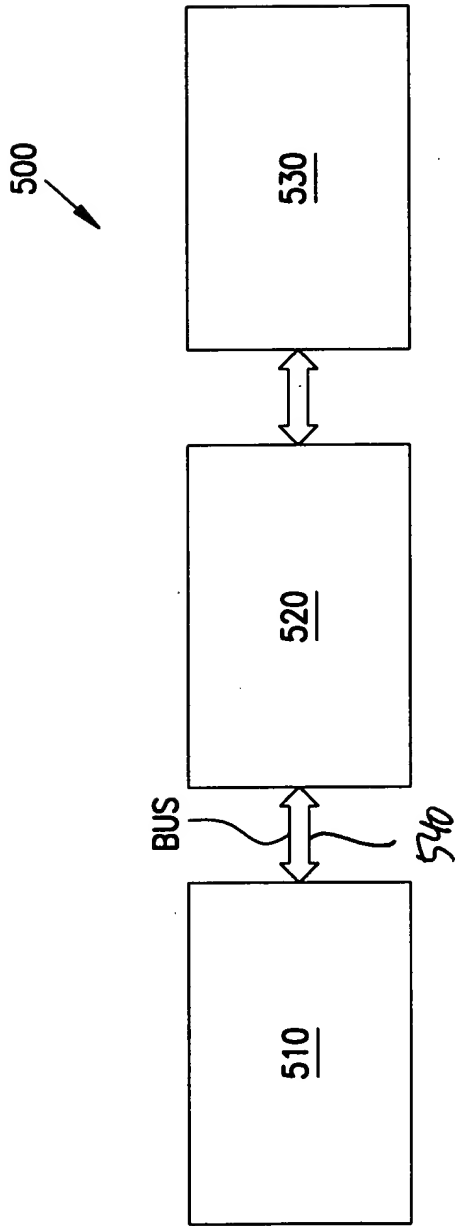


FIG. 11